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(71) Applicant: ADVANCED CHEMICAL SYSTEMS INTERNATIONAL, INC. [US/US]; 510 Alder Drive, Milpitas, CA 95035 (US).

(72) Inventors: BREWER, Richard; 1450 Almaden Valley Drive, San Jose, CA 95120 (US). GREBINSKI, Thomas, J.; 1920 Tallwood Lane, Boise, ID 83706 (US). CURRIE, James, E.; Route 1, Hammond Hill Road, Box 47C, Dover Plains, NY 12522 (US). JONES, Michael; 484–3 Madera Avenue, Sunnyvale, CA 94086 (US). MULLEE, William; 10592 S.W. 63rd Drive, Portland, OR 97219 (US). NGUYEN, Ann; 3846 Glengrove Way, San Jose, CA 97219 (US).

(74) Agents: FLIESLER, Martin, C. et al.; Fliesler, Dubb, Meyer and Lovejoy LLP, Suite 400, Four Embarcadero Center, San Francisco, CA 94111–4156 (US).

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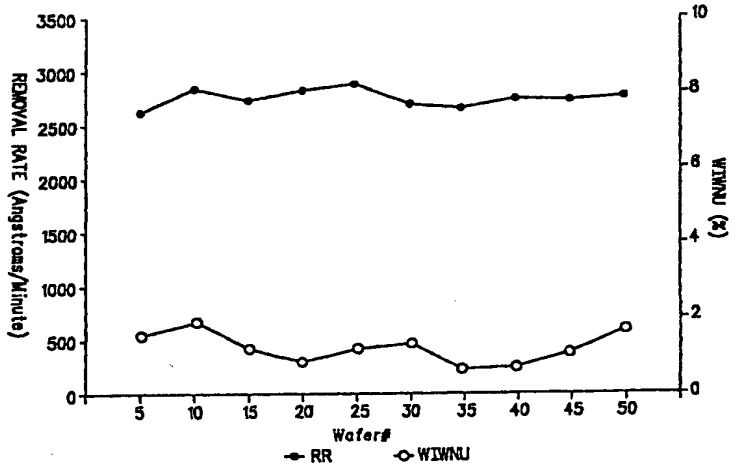

(57) Abstract

A planarization composition is set forth for chemical mechanical planarization of dielectric layers for semiconductor manufacture. The composition comprises spherical silica particles having an average diameter of from 30 nm to about 400 nm, and a narrow range of particle sizes, wherein about 90 % of the particles is within 20 % of the average particle diameter. The composition includes a liquid carrier comprising up to about 9 % alcohol and an amine hydroxide in the amount of about 0.2 to about 9 % by weight. The pH of the composition is in the range of about 9 to about 11.5, and the remainder of the solution is water. The composition has low amounts of metal ions, and the composition is used for thinning, polishing and planarizing interlayer dielectric thin films, shallow trench isolation structures, and isolation of gate structures. The invention also comprises methods for using the planarization composition in the manufacture of semiconductor devices.

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PLANARIZATION COMPOSITIONS FOR CMP OF INTERLAYER DIELECTRICS

BACKGROUND OF THE INVENTION

I. Technical Field

The present invention relates to a planarization composition which is particularly useful for thinning, polishing and planarizing integrated circuitry deposited on semiconductor wafers which have an inter-layer dielectric material deposited on their surfaces to form insulating dielectric films. The thinning, polishing and planarizing serves to remove a portion of the dielectric film so as to flatten and smoothen the deposited dielectric surface, and further to remove excess deposited dielectric material during the formation of shallow trench isolation structures. The invention also relates to a thinning, polishing and planarizing apparatus and method for carrying out the thinning, polishing and planarizing process to flatten and smoothen the dielectric film and to remove excess deposited dielectric material during the formation of shallow trench isolation structures.

II. Discussion of Related Art

In semiconductor processing, it is common to deposit a thin film of an insulating material, for example a dielectric such as doped or undoped oxides of silicon, over already existing dielectric thin films interspersed with other exposed semiconducting and conducting integrated circuit features such as a semiconductor trenches lined with a thin thermal oxide and high density plasma oxide, tungsten silicide/polysilicon/gate structures or titanium/aluminum/titanium nitride structures. The deposited insulating thin

film acts as an electrical isolation layer between semiconductors and conducting pathways adjacent to and under the insulating thin film. The deposited material constitutes what is commonly referred to as a shallow trench isolation structures or an interlayer dielectric insulator. When this process is carried out, a thin coating of the material being deposited to fill, and therefore electrically isolate, the semiconductor and inter-gate and inter-metal gaps is deposited globally on the upper surface of the remaining exposed insulating thin films, semiconducting and conducting pathways. The deposited dielectric material is deposited to sufficiently fill the gaps between adjacent semiconducting gate structures and metal conducting pathways, thus partially planarizing the upper surface.

For shallow trench isolation and gate structures, it is preferable to fill the gaps and continue to deposit the dielectric so that there is an excess amount of dielectric material deposited substantially above the gaps. This process is commonly called a gap-fill process. Depending on the type of integrated circuit there may be from one to three types of dielectric materials deposited to complete the gap-fill process, such as the thermally grown and high density plasma CVD deposited oxides used for shallow trench isolation. Each type serves a unique purpose. However, after this dielectric gap-fill process, the planarity of the resultant gap-filled surface is not planar enough to be used as an imaging plane upon which the next pattern of circuitry is defined by photolithographic techniques. A surface that is not highly planar and that has a high scratch density and surface roughness will yield circuit features of varying degrees of quality that will have direct impact on device performance and yield. This is due to the non-planar scratched and rough regions being "out-of-focus" relative to the planar unscratched and smooth regions. Thus, this non-planar dielectric surface must be planarized and surface roughness

and scratches be reduced further prior to carrying out the IC patterning process.

The removal of layers of this nature is generally carried out by a thinning, polishing and planarizing operation utilizing a hard surface of a polishing pad and a polishing slurry which wets the pad and is frictionally moved against the excess deposited dielectric surface to be removed. The slurry generally includes silica particles as the abrasive material along with a liquid carrier. Basically, the silica and the liquid carrier are respectively hard enough so as to abrade away the still unplanarized dielectric thin film. The aforementioned method planarizes by mechanical means only. The result, however, is a planarized surface that has a substantial number of scratches and a surface roughness that is not suitable for the manufacture of integrated circuits which utilize sub 0.35-micron geometries. Further, in addition to the polishing and planarizing rates for this method being too low to be production-worthy, this type of thinning, polishing and planarizing slurry is considered too dirty having high levels of potential yield-limiting metal ion impurities incorporated in the liquid carrier and the silica slurry abrasive.

It is well known to combine the abrasive and liquid carrier with a reactive chemical constituent. This method is commonly referred to as chemical mechanical polishing (CMP). In this process, more rapid thinning, polishing and planarizating can occur through utilization of an abrasive material, generally alumina or silica, along with a liquid carrier and a compound which is corrosive or oxidative toward or will dissolve the substrate. For example, U.S. Patent No. 5,391,258 of Brancaleoni, et al. discusses such a process for enhancing the polishing rate of silicon, silica or silicon-containing articles including composites of metals and silica. The composition includes an oxidizing agent along with an anion which suppresses the rate of removal of the relatively soft silica thin film. The suppressing

anion may be any of a number of carboxylic acids. Alumina is used as the abrasive material.

It is also known to utilize another abrasive material, specifically silica of very small size, to polish substrates such as rough cut silicon wafers prior to beginning their processing into integrated circuit devices. As an example, Shimizu, et al., in U.S. Patent 4,842,837, teaches a process for producing fine spherical silica having a particle size of 0.5 m and less. The particles are mono-dispersed whereby polishing of the relatively soft, chemically reactive silicon wafer surface can be carried out to produce a substantially flat wafer surface. The resulting colloidal silica was proposed as a polish for silicon wafers, specifically silicon wafers but not interlayer dielectrics such as doped and undoped thermally grown or CVD deposited oxides of silicon. Further, the resulting colloidal silica had unacceptably high ammonia and alcohol contents that prohibited them from being used broadly in silica wafer polishing and frm being used for interlayer dielectric and shallow trench isolation CMP.

U.S. Patent No. 5,376,222 discloses the use of colloidal silica in an alkaline solution for polishing a silica film on a semiconductor. The polishing solution includes a cation of an alkali metal, an alkaline earth, or an ammonium ion.

U.S. Patent No. 3,877,183 discloses the use of precipitated silicates and/or silicofluorides as polishing substances for semiconductor materials. These polishing substances are utilized to polish the semiconductor, namely, silicon.

A very real problem exists with respect to polishing materials such as insulating dielectric films without scratches and sufficiently low enough surface roughness and post-planarization surface and dielectric film cleanliness. Insulating thin films are deposited within the channels which fills

the channels but still leaves the dielectric thin film surface not planar enough. Further, insulating thin films are deposited to substantially fill shallow trenches. The trenches are intentionally over-filled and then polished and planarized back to the plane of the filled trench. So, what is commonly referred to as a planarization process, is implemented to remove, layer by layer, the "bumpiness" of the dielectric thin film, and to remove the globally deposited oxide trench over-fill back to the plane of the oxide filled trench.

Today's state of the art planarization process, although at one time was sufficient enough to fully planarize the dielectric surface, is no longer sufficient. Scratches (macro-scratches) and haze (micro-scratches and light-point defects), which were once not considered yield-limiting defects, are considered yield-limiting defects today and today's benign scratches and haze most likely will become more substantial yield-limiting factors with tomorrow's more advanced, higher performance, integrated circuits. Relatively speaking, planarized and polished dielectric surfaces must be smoother, cleaner, scratch-free and more planar than they are today. Particle size distribution and the shape of the abrasive are the two of the most important factors which affect scratch density and haze. Today's abrasives used for dielectric planarization are almost exclusively fumed silica whose particle size distribution and shape cause undesirable surface scratches and haze. The particle size distribution of fumed silica and alumina can range from 24 to greater than 300 percent. More recently, the industry has been testing precipitated silicas, as opposed to fumed silicas, for dielectric CMP. With precipitated silica slurries the surface roughness and scratch levels are substantially improved over fumed silicas but today's commercially available and most widely used are manufactured from sodium silicate or potassium silicate. Sodium and potassium are considered the most dangerous yield-limiting contaminants to integrated circuits during their manufacture and

therefore the use of precipitated silicas have not gained industry-wide acceptance. Further, there are other high levels of yield-limiting impurities in precipitated silica slurries such as alkaline earth, transition metal and heavy metal ions that make precipitated silicas undesirable as a thinning, polishing and planarizing dielectric slurry. Because today's fumed silica and alumina slurries are so dirty, an extensive and costly post-thinning and planarizing cleaning process must be implemented to remove only some of the slurry-induced, yield-limiting surface and sub-surface impurities.

At the start of a typical prior art thinning and planarizing (CMP) process, one or more dielectric layers are exposed. After a substantial amount of thinning, polishing and planarization, the bumps and oxide overfill remaining are sufficiently removed so as to produce a planarized surface. With the conventional fumed silica-based thinning and planarizing process, the dielectric surface is planarized while scratches, haze and surface impurities remain on the surface. For instance, the most widely used slurry thins and planarizes with a particle size distribution of 23 to 300 plus percent and impurity levels exceeding 50,000 ppb. The result of the thinning and planarizing process is an unpredictably rough and scratched surface that has unacceptably high levels of surface and sub-surface yield-limiting impurities such as sodium, potassium, aluminum, iron, and chlorides.

Integrated circuit manufacturers have been asking fumed and precipitated silica slurry manufacturers to improve today's slurry particle size distribution and purity but without much success. Although the fumed silica abrasive has higher purity than today's seldom used precipitated sodium silicate slurry, it does not have the narrow particle size distribution that can be achieved with a precipitated sodium silicate slurry. With a sodium silicate slurry, particle size distributions can be less than 10 percent, thus yielding a much improved surface haze and scratch density, but this improved performance is

accomplished at a relatively inferior impurity concentration level. Especially for the CMP of shallow trench isolation structures, such as a sodium or potassium silicate slurry has the potential to degrade device yield more substantially than any defects traceable to surface scratches and haze. Thus today's precipitated silica slurries, based on sodium silicate, have not gained substantial market acceptance.

To date, there has not been a satisfactory solution to the future need for improved surface roughness, reduced scratch density and improved slurry purity for interlayer dielectric thinning and planarization.

Today's conventional fumed silica and alumina-based dielectric thinning and planarizing slurries have a broad particle size distribution from ± 24 percent to ± 300 plus percent. The higher the particle size distribution, the greater the surface roughness and scratches. Integrated circuit manufacturers are finding today that they must reduce particle size distribution because of a future requirement that they use photolithography technology having a shallower depth of focus. Having a requirement for a shallower depth of focus in the future also requires that the surface of the integrated circuit, as it is being manufactured, have improved surface roughness and less scratches. Any one of the above parameters, if not improved, can cause future, more advanced integrated circuits to fail. To date, there has been a substantial effort to reduce the particle size distribution and therefore reduce haze, improve surface roughness and reduce scratch density but without the substantial success required to meet tomorrow's performance requirements (depth of focus) dictated by photolithography.

Furthermore, because of the still high impurity levels in today's conventional fumed silica slurries, it has been shown that they cause defects and circuitry failure. Further, it has been shown that the higher the purity of the slurry, the lower the normalized integrated circuit defect density.

Accordingly it would be highly desirable to develop a polishing composition which is of a higher purity in order to reduce the post thinning and planarization integrated circuit defect density.

Because of the above shortcomings of today's conventional silica-based thinning and planarizing dielectric CMP slurry, the industry has been looking for an improved thinning and planarizing system which leads to improved surface roughness scratch density and slurry purity, while maintaining the same degree of safety. Although an alkosol has the particle size distribution and purity levels consistent with the what will be required by tomorrow's more advanced integrated circuit technology, the polishing rates are to low to be production-worthy. Further, the current alkosols contain at least 30 wt percent of alcohol which is a concentration too high to be used safely in an integrated circuit manufacturing plant. Therefore, the current alkosols, once believed to be the answer, suffer from productivity and safety shortcomings.

OBJECTS OF THE INVENTION

The present invention is directed to overcoming one or more of the problems as set forth above.

Thus, one object of the invention is the manufacture of a spherical alkylsilicate particle for chemical mechanical polishing of semiconductor dielectric materials.

An additional object of the invention is the manufacture of alkylsilicate particles for chemical mechanical polishing, which have narrow size distributions.

A further object of the invention is the manufacture of alkosol based alkylsilicate slurries with reduced amounts of alcohols while maintaining low metals content and narrow particle size distribution.

Another object of the invention is the manufacture of alkylsilicate slurries permitting decreased surface roughness, decreased scratches and decreased haze of semiconductor dielectric films.

An additional object of the invention is the development of methods for manufacturing alkylsilicate based slurries having reduced alcohol and high purity for higher planarization rates.

A yet further object of the invention is the development of planarization compositions which are of very high purity with low alcohol content.

A yet additional object of the invention is the development of planarization compositions which are of very high purity with reduced ammonia concentrations.

Another object of the invention is the development of planarization compositions with very low metal contamination.

A further object of the invention is a method for planarizing dielectric semiconductor surfaces with high planarization rates, low within-wafer non-uniformity and low surface roughness.

Yet another object of the invention is the optimization of the polishing process to achieve desired rates of polishing and desired surface roughness, while maintaining a high margin of safety during use.

Another object of the invention is the manufacture of semiconductor devices incorporating the planarization compositions and methods.

Therefore, the invention comprises methods for manufacturing highly purified, low alcohol alkosol-based alkylsilicate slurries made by the alkaline hydrolysis of alkoxysilane precursors in aqueous, alcoholic, basic solutions.

Thus, one aspect of the invention is the manufacture of a spherical alkylsilicate particle for use in chemical mechanical polishing.

An additional aspect of the invention is the manufacture of alkylsilicate particles which have narrow size distributions.

A further aspect of the invention is the manufacture of alkosol based alkylsilicate slurries with reduced amounts of alcohols.

A yet additional aspect of the invention is the development of planarization compositions which are of very high purity with reduced ammonia concentrations.

Another aspect of the invention is the manufacture of alkylsilicate slurries permitting decreased surface roughness of semiconductor dielectric films.

An additional aspect of the invention is the development of methods for manufacturing alkylsilicate based slurries for improved planarization.

A yet further aspect of the invention is the development of planarization compositions which are of very high purity.

Another aspect of the invention is the development of planarization compositions with very low metal contamination.

A further aspect of the invention is a method for planarizing dielectric semiconductor surfaces with high planarization rates, low within-wafer non-uniformity and low surface roughness, while maintaining a high margin of safety during use.

Yet another aspect of the invention is the optimization of the polishing process to achieve desired rates of polishing and desired surface roughness.

Another aspect of the invention is the manufacture of semiconductor devices incorporating the improved planarization compositions and methods.

SUMMARY OF THE INVENTION

This invention comprises new ways of manufacturing ultra-high purity alkylsilicate particles and alkylsilicate slurries having low alcohol content for chemical mechanical planarization (CMP), new compositions for CMP, and semiconductor devices incorporating the use of the new compositions and

methods. Alkylsilicate particles are made by the alkaline hydrolysis of alkoxysilane precursors in aqueous solutions. By selecting appropriate conditions of hydrolysis and condensation of silicates into alkylsilicate, it is possible to achieve unexpectedly low surface roughness, few scratches and reduced surface haze at sufficiently high polishing, thinning and planarization rates. Further, the conditions of slurry manufacture can be selected to optimize polishing rates and surface roughness to achieve the desired film quality and throughput of semiconductor wafers during manufacturing. The compositions and methods are valuable in the manufacture of semiconductor devices with high feature density, thereby permitting the manufacture of semiconductor products with increased speed, reliability, and at lower power and cost.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the figures of the drawings wherein like numbers denote like parts throughout and wherein:

Figure 1 illustrates a schematic view of a pad being wet by the planarization composition of the present invention.

Figure 2 illustrates a pad in accordance with the embodiment of the present invention wet by a composition in accordance with the present invention in position to thin, polish and planarize a hard flat surface layer from a partially fabricated integrated circuit.

Figure 3 illustrates the rubbing of the pad of Figure 1 across the hard flat surface layer of Figure 2 for providing the desired thinning, polishing and planarizing.

Figure 4 is a graph depicting polishing rates and within-wafer non-uniformity of polishing thermal oxide wafers using low alcohol compositions of the invention.

Figure 5 is a cross-sectional view illustrating a sample semiconductor device manufactured using the method for manufacturing gate structure and inter-layer dielectrics before planarization of the present invention.

Figure 6 is a cross-sectional view illustrating a sample semiconductor device using the method for manufacturing gate structure and inter-layer dielectrics after planarization of the present invention.

Figure 7a is a depiction of a shallow trench isolation before CMP.

Figure 7b is a depiction of a shallow trench isolation after CMP of this invention.

DETAILED DESCRIPTION OF THE INVENTION

This invention provides compositions and methods for chemical mechanical planarization of semiconductor surfaces. The compositions comprise alkylsilicate particles in aqueous suspensions containing an alcohol, water, and a base. The compositions are used with equipment to polish semiconductor dielectric surfaces to achieve films of high surface purity, high within-wafer uniformity, and decreased surface roughness and decreased haze.

I. Alkosol Based Precipitated Alkylsilicate Slurry

As used herein, the term alkosol means an aqueous suspension of alkylsilicate particles made by the hydrolysis of an alkoxysilane under alkaline conditions, in the presence of an alcohol. This invention comprises alkosol slurries for chemical mechanical planarization which comprise precipitated alkylsilicate particles in an aqueous, alcoholic, ammoniacal medium. Embodiments of the compositions also comprise low alcohol and/or low amine slurries which exhibit higher polishing rates and lower within-wafer non-uniformity than higher alcohol and/or amine compositions. The compositions comprise spherical alkylsilicate particles having a alkylsilicate

particle concentration of 0.5 to 30 weight percent, a weighted average particle diameter which falls within the range from about 0.4 μm to about 0.03 μm, and is mono-disperse in that at least about 90 weight percent of the particles have a variation in particle diameter from the average particle diameter of no more than about $\pm$ 20 %. A liquid carrier comprises up to about 9 weight percent ROH, and an amine hydroxide which is NR_4OH or NR_2NR_3OH, where each R is any one of H, HCH_3, CH_2CH_3, C_3H_7 or C_4H_9, in the amount of about 0.2 weight % to about 10 weight %, the balance of the mixture being water.

We have unexpectedly found that reducing the alcohol concentration to the range of about 0 weight % to about 9 weight % substantially increases the polishing rates for the slurries of this invention compared to levels obtained using higher concentrations of alcohol. Moreover, further decreasing the alcohol concentration results in an unexpected further increase in polishing rates. Slurries with these lower alcohol concentrations provide higher polishing rates than currently available alkosols.

The following Table 1 shows some of the differences between slurries comprising fumed silica and precipitated silica of the prior art and the planarization composition of the invention.

Table 1

Physical and Chemical Characteristics of Slurries for Dielectric CMP

Variable	Prior Art Fumed Silica	Planarization Composition of the Invention
Metal Ion Contamination (ppb)	50,000	2000
Particle Size Distribution (%)	23-300	5-20
Abrasive Type	branched-chain agglomerate (non-spherical)	monodisperse spherical

The ammoniated TEOS alkylsilicate particles of this invention are spherical and monodisperse (of a uniform size and within a specific and limited size range and chemical composition and purity). The particles are used in a slurry to controllably polish hard materials and produce a resultant polished surface which is highly planar, relatively smooth and relatively metal ion free, scratch free and therefore defect-free.

When an hydroxyl amine, such as ammonium hydroxide, is present in the composition slurry mixture at weight percentages between 0.2 and 9.0 weight percent, thinning and planarization rates similar to those obtained using conventional fumed silica and precipitated silica slurries are realized. Unexpectedly however, reducing the concentration of the hydroxyl amine to below about 4 weight % increases the polishing rates substantially above those obtained using slurries with higher hydroxyl amine concentrations. Thus, preferred concentrations of hydroxyl amines are in the range of about 0.2 weight % to about 4 weight %, respectively. These concentrations of amines help to

provide a pH of the final composition between about 9 to about 11.5, preferably between about 10 and about 11.5, and more preferably between about 10 and 11.

However, surprisingly, the high polishing rates are achieved with about only one-half the surface roughness levels, measured as the root mean square (rms) in Å, one-tenth the density of scratches larger than 1 μm long and greater than 1 μm deep, about ½ the surface roughness, and a substantial reduction of the post-CMP particle and residue levels encountered after thinning with the conventional silica-based slurries.

II. Manufacture of Alkosol Based Precipitated Silica Slurries

The manufacture of the alkosol based precipitated silica slurries of the invention comprise the hydrolysis of a precursor, such as TEOS, in an ammoniacal solution with alkaline pH, and the subsequent reaction whereby the reactive intermediate silicates condense to form alkylsilicate particles. The final compositions of the slurries can then adjusted before use, through the removal of alcohol and raising or lowering the pH of the resultant slurry composition.

A. Alkaline Hydrolysis of Alkoxysilane Precursors

The hydrolysis of alkoxysilane precursors in this invention occurs in an alkaline environment. By way of example only, the discussion which follows describes the reactions wherein the alkalinity is maintained by ammonium hydroxide.

An aqueous solution of ammonium hydroxide has five components: H_2O, H_3O^+, OH^-, $NH_3(aq)$, NH_4^+. When combined with a silica precursor such as TEOS and water, there are at least two mechanisms for the hydrolysis, of which those for TEOS are described below:

$(EtO)_4Si$ (TEOS) + $4H_2O$ → $Si(OH)_4$ + 4EtOH Reaction 1

$Si(OH)_4$ → SiO_2 + $2H_2O$ Reaction 2

and $(EtO)_4Si + 4OH^-$ → $Si(OH)_4 + 4EtO^-$ Reaction 3

$EtO^- + NH_4^+$(or H_3O^+) → EtOH + NH_3 (or H_2O) Reaction 4

and $Si(OH)_4$ → SiO_2 + $2H_2O$ Reaction 5

At this point, the components in the system are H_2O, $(EtO)_4Si$, H_3O^+, OH^-, NH_3(aq), NH_4^+, EtOH, and SiO_2. The above reactions represent only possibilities for the formation of the alkylsilicates of the invention. Other chemical reactions and theories may also result in the production of alkylsilicates from the precursors, and all are considered to be part of the invention. Other alkoxysilane precursors are well known in the art, and any of them are suitably used in this invention. The only criterion for selecting other alkoxysilane precursors is that the alcohol liberated during hydrolysis be compatible with the semiconductor dielectric and other features, such as conductive metal lines and relatively safe for use in an integrated circuit manufacturing facility. Even precursors with incompatible alcohols can be used in this invention if the alcohol can be removed to the desired degree after the hydrolytic and condensation reactions have taken place.

In accordance with a particularly preferred embodiment of the invention, the materials utilized are all of ultra-pure quality whereby the suspension has a total metals content of no more than about 20,000 parts per billion by weight, preferably no more than about 2000 parts per billion by weight, and more preferably, no more than about 500 parts per billion by weight. This is particularly useful in the semiconductor processing industries since even small

amounts of metal ions in dielectric films can cause errors in devices thereby reducing device reliability and yield.

B. Manufacture of Alkylsilicate Slurries

The methods of formulating the silica particles involve the alkaline hydrolysis of an alkoxysilane precursor and the condensation of the silicate intermediates to form SiO_2 and the resulting alcohol. Generally, any alkoxysilane precursor can be used, but tetraethylorthosilicate (TEOS) is the preferred precursor. Additionally, the hydrolysis reaction can be catalyzed by raising the pH to above about 7 using any convenient, metal-free base solution. However, ammonium hydroxide is preferred. The resulting solution comprises alcohol, ammonia, and water. The products formed by the reaction include the silica particles of the desired size, ammonia, ammonium ions and the alcohol corresponding to the alkoxysilane used. What results is a suspension of spherical silica particles in an alcoholic ammonium hydroxide solution.

The reactants and reaction conditions can be varied. For example, the TEOS can be replaced with any tetraalkylorthosiloxane, wherein the leaving group is compatible with the manufacturing processes and the final products. By way of example only, the alkyl groups can comprise methyl, propyl or butyl moieties. If this is done, the product is not ethanol but instead is the corresponding alcohol. It is not necessary that the precursor have four identical alcoholic leaving groups. Thus, methylethylbutylpropylorthosiloxane is suitable in any of its structural isomers. Similarly, many other precursors with appropriate combinations of alcoholic leaving groups can be used in this invention.

Generally, the final alcohol constituent of the slurry may be from about 0 weight % up to about 9 weight %. However, for certain applications, it is

desirable for the alcohol concentration to be reduced to lower than about 4 weight %. Reducing the alcohol content of the slurry not only results in increasing polishing rates, but unexpectedly improves the planarity of wafers, as reflected in decreased % within-wafer non-uniformity. As a general method, the concentration of alcohol in the final composition can be adjusted by evaporation or by ultrafiltration (UF). If TEOS is used as a silica precursor, the resulting alcohol (ethanol) can be evaporated by heating during the slurry manufacturing step. Furthermore, other alcohols with low vapor pressure can be removed by evaporation. However, for both ethanol and alcohols with higher vapor pressures than ethanol, other methods such as ultrafiltration can be used. It is desirable to use a UF system which is resistant to corrosion by the chemicals used. By way of example only, the Graver UF system is made of titanium oxide and type 316 stainless steel, which are relatively resistant to corrosion, and is relatively non-contaminating.

It is generally desirable to allow the alkylsilicate particle formation steps to reach completion before removing the alcohol and amine. The remainder of the composition is water, preferably of ultra-high purity (containing no more than about 5 parts per billion). It is desirable for the total amount of water to not exceed about 70% by weight.

The ammonium hydroxide can be replaced by potassium hydroxide or compounds of the formulas NR_4OH, and/or NR_2NR_3OH where each R is any one of CH_3, CH_2CH_3, C_3H_7 or C_4H_9. The amine hydroxide constituent of the nature defined above will usually be present in the amount from about 0.2% to about 9 weight %. It is preferable to have reduced ammonium hydroxide levels, typically in the range of about 0.2 weight % to about 4 weight %. Generally, the ammonium hydroxide can be removed using ultrafiltration or evaporation methods. After removal of a first base, the pH can be adjusted by

adding a second base to the slurry. This permits the removal of ammonium hydroxide, which in some applications can be undesirable, and replacing it with potassium hydroxide or other suitable bases to keep the pH in the desired range.

In accordance with the present invention, the pH is adjusted to be within a range from about 9.0 to about 11.5, preferably between about 10 and about 11.5, and more preferably from about 10 to about 11 This pH range provides the necessary ammonia contents necessary to achieve favorable thinning and planarizing rates. It is not desirable to make the composition too neutral (pH about 9.0 or less) or too basic (above about 11.5), because the thinning and planarizing rates decrease to unacceptably low levels.

By carefully adjusting the pH of the alkosol slurry, one can optimize the rate of removal of dielectric materials with respect to the ultimate surface roughness achieved by the planarization process required for integrated circuit manufacture. We have found that by adjusting the pH and alcohol content, fine gradations in polishing rates and surface roughness can be achieved (see Examples 6-7, and 9-10 below). This sensitivity of polishing rate and surface planarization was not appreciated by any of the prior art methods using an alkosol based slurry. Suitable acids which may be used to adjust the pH include acetic acid, nitric acid, citric acid, hydrochloric, carboxylic, acetylsalicylic or sulfuric acid.

Generally, higher rates of dielectric removal result in greater surface roughness. Generally, it is preferred that the amount of NR_4OH, alcohol, alkylsilicate content and the pH are selected such that surface polishing rates of dielectric materials are, for BPTEOS, above 500 Å/min to about 15,000 Å/min, preferably between about 3000 Å/min and about 15,000 Å/min, and for thermal oxide, the typical polishing rates are between about 500 Å/min and about 10,000 Å/min, preferably between about 1500 Å/min and about

10,000 Å/min. The desired root mean square surface roughness is in the range of below about 20 Å, preferably below about 10 Å, and more preferably, below about 5 Å.

II. Use of Ammoniacal Alkylsilicate Slurries for CMP

In accordance with another embodiment of the present invention, a pad which is wet with the above planarization composition is set forth. Additionally, another embodiment of the invention is a method of planarizing a substrate having an insulating surface coating to remove the coating. The method comprises positioning the planarization composition set forth above between a pad and the surface coating and rubbing the pad against the surface coating until the surface coating has been removed.

A. Formation of Electrically Isolated Gate Structures

Yet another embodiment of the invention is a method for electrically isolating gate structure structures. By way of example only, a thin 50 Å - 200 Å silicon dioxide layer is grown globally over a partially completed integrated circuit. Next, a thin film of polysilicon is deposited onto the thin, thermally grown, gate oxide. Further, a silicide film is deposited globally onto the polysilicon thin film. The silicide can be any suitable silicide, and includes, by way of example only, titanium silicide, tantalum silicide, and tungsten silicide. The three grown and deposited thin film layers form the material needed for what is referred to as a gate structure. Next, the surface is patterned with photoresist, etched, and stripped, leaving behind very small sub-micron sized islands of gate structures. On a typical microprocessor 0.5 by 0.5 inches per side, there may be as many as 10,000,000 gate structures. Further, the regions between the islands of the gate structures are filled with what is commonly referred to as an interlayer dielectric insulator. The

dielectric insulator fills the gaps and electrically insulates one gate region from another. After the gap filling process, the integrated circuit surface is smoother and more planar because the regions between the gate structures have been substantially filled with a dielectric such as a doped or un-doped oxide of silicon. A planarizing composition as set forth above is positioned between the inter-layer dielectric surface and a pad. The pad is rubbed against the inter-layer dielectric surface sufficiently to thin and planarize any microscopic bumps on the wafer surface.

B. Manufacture of Interlayer Dielectric Materials.

In another embodiment of the invention, devices containing interlayer dielectric materials, metals, and barrier materials are manufactured by providing a substrate with a dielectric layer, such as by way of example only, a CVD oxide, then providing a patterned photoresist layer, wherein the first dielectric layer is partially exposed. Then, the dielectric surface is etched to form one or more small holes in the dielectric layer, the etching step accomplished, by way of example only, using plasma etching, followed by a photoresist stripping step. Subsequently, a barrier layer is deposited, followed by the deposition of a metal layer. Then, the surface is planarized and thinned to remove excess metal and barrier layer, thus exposing the dielectric layer and the filled holes.

C. Shallow Trench Isolation

To manufacture shallow trench isolation structures, a substrate of epitaxial or bulk silicon is coated with a silicon nitride CMP stop layer. Subsequently, the stop layer is patterned with photoresist, leaving the surface at least partially exposed, followed by an anisotropic plasma etch step of both the stop layer and the underlying substrate, forming at least one small hole. A

thin layer of thermal oxide is grown to coat the inside sidewalls and bottoms of the holes, followed by the deposition of a layer of dielectric material, which substantially fills the holes. The excess dielectric material, above the plane of the first surface is then thinned and substantially planarized using CMP methods of this invention.

D. Planarization Methods

Operating in accordance with the invention, any dielectric material, silicide or barrier layer can be planarized using the compositions of this invention. By way of example only, such common dielectric materials as Boron-Phosphorous-doped Silicate Glass (BPSG), Phosphorous-doped Silicate Glass (PSG), Phosphorous-doped Tetraethylorthosilicate (PTEOS), Thermal oxide, Tetraethylorthosilicate (TEOS) oxides, Plasma Enhanced Tetraethylorthosilicate (PETEOS) oxides and high-density plasma CVD (HDPCVD) oxides can be thinned and planarized by the above disclosed slurry formulation. Silicides include tantalum silicide, titanium silicide and tungsten silicide.

When thinning and planarizing inter-layer dielectrics, it is desirable to remove by polishing, thinning and planarizing the dielectric thin film to render the film perfectly planar with low surface roughness and low scratch density and still have remaining excess dielectric material covering the gate structures and other conducting and semiconducting integrated circuit features. Further, when thinning and planarizing oxides are used for shallow trench isolation, it is desirable to polish back to either the CMP stop layer, typically a silicon nitride, or back to the epitaxial silicon or bulk silicon surface that is coplanar with the top of the oxide filled shallow trench.

Planarizing is accomplished by positioning the planarization composition described above between the pad and the surface coating of the wafer. In this

embodiment, dielectric thin film with the dielectric surface is contacted with the pad wet with the aforementioned composition. The pad is rubbed against the second metal surface due to the rotation of the wafer.

The temperature for the thinning, polishing and planarizing operation will generally fall within a range from about 20°C to about 80°C. Indeed, the operation is generally initially at about 20-50°C but the temperature of the surface and the liquid carrier goes up as friction takes place.

Once the dielectric layer is sufficiently planarized, the surface can be subjected to further processing steps, including, but not limited to post-CMP surface cleans, photolithography, anisotropic plasma etching, and the application of barrier layers, metal plugs and vias. The metal plugs and vias typically comprise tungsten, aluminum or copper. The barrier layers are typically titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride and titanium/tungsten.

The invention will be better understood by reference to the following illustrative experimental examples which demonstrate some of the compositions, methods of manufacture, methods of use, and advantages of the invention.

EXAMPLES

In the following Examples 1 - 4, methods for synthesizing slurries for CMP are described using alcoholic alkaline hydrolysis of the silica precursor, tetraethylorthosilicate (TEOS). The concentration of each starting material in each starting solution is included in parentheses. Other examples show the use of the slurries and methods of this invention to achieve improved polishing characteristics for dielectric thin films.

Example 1: Method 1 for Manufacturing Ethyl Silicate Slurry

1. Materials

Solution A: 73 milliliters (ml) 28 % ammonium hydroxide (NH_4OH; concentration: 2.07 mol/l)
41 ml water (H_2O; concentration: 26.94 mol/l)
8 ml ethyl alcohol (ETOH; concentration: 0.16 mol/l)

Solution B: 46 ml TEOS; (final concentration: 1.92 mol/l).

2. Synthesis of Primary Particles

a. Warm a beaker to 33° C to 37° C.

b. Add solutions A and B dropwise over 15 minutes, with constant stirring at 280 rpm into beaker with the flow rate of A twice the flow rate of B.

c. remove from heat, stir, cool to 21.5° C over 15 min.

3. Growth of Final Particles

a. Warm solution to 35° - 37° C while adding dropwise with stirring: 250 ml TEOS and 394 ml H_2O.

b. Stir for 1.0 hours in a closed vessel.

c. Add 30 ml TEOS dropwise every 30 minutes for a total of 3 additions.

d. Particle size: 160 - 180 nm.

4. **Final Slurry Composition** **(weight percent of total)**

   a. 12.95% silica (SiO_2)

   b. 2.0% NH_3

   c. 40.35 % ETOH

   d. 44.7% H_2O.

   e. Particle size: 170 $\pm$ 15 nanometers (nm; 8.8% standard deviation; "SD")

Example 2: Method 2 for Manufacturing Ethyl Silicate Slurry

1. **Materials**

   a. Solution A: 123 ml of 28 % NH_4OH;
   (concentration: 6.96 mol/l)
   60 ml H_2O; (concentration: 19.78 mol/l)
   10 ml ETOH; (concentration: 0.31 mol/l)

   b. Solution B: 24 ml 28% NH_4OH and 133 ml H_2O.

2. **Synthesis of Primary Particles**

   a. Pre-warm beaker to 33° C to 37° C.

   b. Add Solution A to beaker dropwise over 30 minutes along with 77 ml TEOS with constant stirring at 280 rpm and flow rate of Solution A being twice the flow rate of TEOS (final TEOS concentration, 1.59 mol/l).

3. **Growth of Final Particles**

   a. To the solution containing primary particles, add Solution B and 115 ml TEOS, both dropwise over 30 minutes, with constant stirring and with the flow rate of Solution B being

twice that of the TEOS. After 2/3 of the TEOS has been added, the heat is turned off.

b. Stir for 1 hour more in a closed vessel.

4. Final Slurry Composition

a.	Silica:	10.11 %.
b.	NH_3:	7.23 %.
c.	ETOH:	32.47 %.
d.	Water:	50.19 %.
e.	Particle size:	170 $\pm$ 22.5 nm (13 % SD)

Example 3: Method 3 for Manufacturing Ethyl Silicate Slurry for CMP

1. Materials

a. Solution A: 147 ml NH_4OH, (concentration: 6.71 mol/l) 72 ml H_20, (concentration: 19.38 mol/l) ml ETOH, (concentration: 0.36 mol/l)

b. Solution B: 124 ml H_2O.

2. Synthesis of Primary Particles

a. Pre-warm beaker to 33° C to 37° C.

b. Add Solution A and 92 ml TEOS over 15 minutes, stir at 280 rpm with the flow rate of Solution A being twice the flow rate of the TEOS solution.
(final TEOS concentration: 1.65 mol/l)

c. Let cool while stirring, over 15 minutes to 21.5° C.

d. Particle size: 160 - 180 nm.

3. Growth of Final Particles

a. Warm the solution containing primary particles to 33° C to 37°.

Cover 30 minutes while adding Solution B and 115 ml TEOS, with the flow rate of Solution B being twice the flow rate of the TEOS. Reduce the heat after 1/3 of the TEOS has been added.

b. Stir in a closed vessel for 1 hour.

c. Particle size: 160 - 180 nm.

4. Final Slurry Composition

a. Silica: 10.51 %.

b. NH_3: 6.97 %.

c. ETOH: 33.97 %.

d. Water: 48.55 %.

Example 4: Method 4 for Manufacturing Ethyl Silicate Slurry for CMP

1. Materials

a. Solution A:

850 ml NH_4OH, (concentration: 5.67 mol/l)

1,200 ml H_20, (concentration: 17.32 mol/l)

800 ml ETOH, (concentration: 3.55 mol/l)

Mix at low speed.

b. Heat Solution A to 50° C.

2. Synthesis of Primary Particles

a. Add 200 ml TEOS, stir on high for 15 minutes.

(final TEOS concentration: 1.17 mol/l)

b. Stir for an additional 10 minutes.

3. Growth of Final Particles

Add 800 ml TEOS dropwise into vortex of stirred solution over 50 to 60 minutes at 50° C.

4. Final Slurry Composition

a.	Silica:	7.65 %.
b.	NH_3:	6.07 %.
c.	ETOH:	41.22 %.
d.	Water:	45.06 %.
e.	Particle size:	100 - 140 nm.

Example 5: Apparatus and Materials for Chemical Mechanical Polishing

The ethyl silicate slurries of this invention can be used to polish BPTEOS and thermal oxide dielectric materials. Figure 1 illustrates a schematic view of a pad **10** being wet with the planarization composition **8** of the present invention. The planarization composition **8** forms a planarization composition thin film **6** on the top surface of the pad **10** to thereby wet the pad **10**. A delivery system **7** brings the planarization composition **8** above the pad **10** which is located on a surface of the polishing platen **60**. Another method of wetting the pad **10** includes a platen (not shown) having holes (not shown) from the top surface of the platen to the bottom surface of the platen. The planarization composition **8** would then be introduced from the bottom surface of the pad **10** through the bottom surface of the holed platen (not shown) to form a uniform planarization composition thin film. It is understood that either method to wet the pad **10** may be used, or any other method, that results in a pad **10** with a uniform planarization composition thin film.

Figure 2 illustrates a schematic view of the pad **10** in accordance with an embodiment of the present invention wet by the planarization composition (not

shown) to form the planarization film **6**. The pad **10** is in a pre-rubbing position **5** before the pad **10** is used to thin, polish and planarize the hard flat surface layer **20** of a partially fabricated integrated circuit (not shown) on wafer **30**. A quill **40**, rotating in a wafer rotating direction **80**, holds wafer **30** in the pre-rubbing position **5** to lower the quill **40** and wafer **30** in the rubbing direction **50** towards the pad **10**. The pad **10** is supported by polishing platen **60** and rotates in a pad rotating direction **70**.

Figure 3 illustrates a rubbing position **90** of the quill **40** and wafer **30** downwardly relative to the pre-rubbing position **5** of Fig. 2. In this rubbing position **90**, the pad **10** wet with the planarization composition to form the planarization composition thin film **6** rubs against the hard flat surface layer **20** of the wafer **30** to provide the desired thinning, polishing and planarizing of the hard flat surface layer **20**. The pad **10** has been wet by a planarization composition of this invention.

To demonstrate the effectiveness of the invention, a planarization composition comprising an ethyl silicate slurry was used, having the following physical and chemical characteristics:

Slurry Composition	
pH	11.1
Weight % (NH_4OH)	2.6
Weight % SiO_2	13.1
Particle size	188 nm
Particle size distribution	13.5 %

The above composition was used to polish semiconductor substrates, BPTEOS (12,000 Å thick), and thermal oxide (6,000 Å thick). The polishing pad was a Rodel model IC1000-A1 CMP device. The example comprises positioning the planarizing composition set forth above between a pad and the

surface coating and rubbing the pad against the surface coating according to the following planarizing parameters:

Polishing Conditions	
Downward Force	9 psi
Back Pressure	4 psi
Table Speed	120 rpm
Quill Speed	80 rpm
Planarizing Time	50 seconds

The amounts of material removed for BPTEOS and thermal oxide were 3,910 Å and 1,018 Å, respectively. The polishing rates for the above thin films were 4,887 Å and 1,272 Å per minute, respectively. Unexpectedly and surprisingly, the within wafer non-uniformities for BPTEOS and thermal oxide were less than 3.5 % and surface roughness for both BPTEOS and thermal oxide were less than 6.0 Å. In contrast with these results, polishing using prior art slurries, resulted in root mean square surface roughness measurements of about 20 Å. Therefore, the compositions and methods of this invention improve the quality of planarization of dielectric films by about 3 fold. These surprising results were completely unexpected based upon the prior art compositions and methods.

Example 6: Use of Ethyl Silicate Slurries for Chemical Mechanical Polishing

A planarization composition was formed using an ethyl silicate slurry having an initial pH and weight percent for the SiO_2 abrasive and ammonium hydroxide as follows:

Slurry Composition	
pH	12.2
Weight % NH_4OH	9.0
Weight % SiO_2	13.1
Particle size	188 nm
Particle size distribution	13.5 %

The pH of the above composition was adjusted by stirring in a partially closed 30 gallon container at room temperature. With elapsed time, the pH of the composition was measured. Samples of the composition were taken at each pH from 12.2 to 11.1, and wafers having BPTEOS and thermal oxide were thinned and planarized. The polishing pad was a Rodel IC1000-A1/Suba IV. The example comprises positioning the planarizing composition set forth above between a pad and the surface coating and rubbing the pad against the surface coating according to the following planarizing parameters:

Polishing Conditions	
Downward Force	9 psi
Back Pressure	4 psi
Table Speed	120 rpm
Quill Speed	80 rpm
Planarizing Time	50 seconds

The polishing rates achieved in this study are summarized in Table 2 below.

Table 2

Effect of Slurry pH on Polishing Rates and Planarity of Oxide Dielectric Materials

pH	BPTEOS Polishing Rate (Å/min)	Thermal Oxide Polishing Rate (Å/min)
12.2	2816	805
12.0	4150	1073
11.8	4463	1193
11.5	4354	1191
11.3	4526	1271
11.1	4772	1301

Example 7: Effects of Slurry pH on Polishing Rates and Planarization of Dielectric Films.

To determine the reproducibility of the polishing by slurries of the invention on planarization, we studied a total of 50 wafers as before, in Examples 5 and 6. A slurry with relatively low pH of the following composition was used:

Slurry Composition	
pH	11.1
Weight % (NH_4OH)	2.6
Weight % SiO_2	13.1
Particle size	188 nm
Particle size distribution	13.5 %

The polishing pad was a Rodel IC1000-A1/Suba IV. The study comprised positioning the planarizing composition set forth above between a pad and the surface coating of CVD oxide and rubbing the pad against the surface coating according to the following planarizing conditions:

Polishing Conditions	
Downward Force	9 psi
Back Pressure	4 psi
Table Speed	120 rpm
Quill Speed	80 rpm
Planarizing Time	50 seconds

50 wafers were thinned and planarized as described. The results obtained for every fifth wafer so treated are shown in Table 3.

Table 3

Reproducibility of Planarization of Dielectric Materials by Ethyl Silicate Slurry

Wafer No.	Removal Rate (Å/min)	Within Wafer Non-Uniformity (%)	Surface Roughness (Ra)
1	4244	2.9	12
5	4436	2.6	8.3
10	4600	3.0	11
15	4843	2.8	10
20	4914	4.5	9.7
25	4848	3.6	8.1
30	4841	3.7	8.8
35	4732	3.6	13
40	4696	3.0	8
45	4543	3.8	12
Mean	**4670**	**3.4**	**9.3**
SD	**203**	**0.6**	**3.5**

The results of Table 3 indicates that the planarization using the slurry of the invention is highly reproducible, with standard deviations (SD) from the mean for the removal rate, within wafer non-uniformity, and surface roughness being 4.3 %, <18 %, and about 31 %, respectively. Although the variability of the within wafer non-uniformity and surface roughness are higher than the variability of the removal rate, the within wafer non-uniformity and surface roughness are substantially lower than the results obtained using prior art slurries.

In contrast with these results, polishing with prior art slurries resulted in root mean square surface roughness measurements of about 20 Å. Thus, the compositions and methods of this invention improve the quality of planarization of dielectric films by about 3 fold. These surprising results were completely unexpected based upon the prior art compositions and methods.

Example 8: Manufacture of Low Alcohol Planarization Compositions

To produce alkosol planarization compositions with reduced alcohol content, a TEOS based silica sol containing a high (35 % - 40 %) ethanol content was first produced, by way of example only, using the methods of Examples 1-4, and then was subjected to an ultrafiltration (UF) process. The UF process removed the excess alcohol and the excess ammonium hydroxide.

A suction side of a pump capable of operating in a flammable materials environment was connected to the source vessel of TEOS-based alkosol slurry. The outlet of the pump was connected to an UF unit. The UF unit was manufactured by Graver Co. It is desirable to use a UF system which is resistant to corrosion by the chemicals used. The Graver UF system is made of titanium oxide and type 316 stainless steel, which is resistant to corrosion, and is relatively non-contaminating.

The slurry was pumped at a temperature of between about 20° C and about 80° C into the ultrafiltration unit and was recirculated back into the supply vessel. Higher temperatures allow the UF process to work more efficiently. Filtrate (permeate) consisting of a mixture of ethanol, ammonium hydroxide, and water was captured and measured for volume as it exited the UF unit. The recirculation and ultrafiltration processes were allowed to continue until the solids concentration increased from an initial 10 % - 15 % to a predetermined, final concentration, typically about 30 %. As the solids concentration increased, the rate of filtrate production decreased. Deionized

(DI) water was added back to the source vessel to dilute the slurry to a pre-determined initial concentration. Recirculation and ultrafiltration continued until the final solids concentration level is reached, whereupon the cycle was repeated.

When the ethanol concentration reached about 4%, the pump was stopped, and the slurry product was diluted to the final concentration using 3% ammonium hydroxide solution.

Slurries of differing alcohol and ammonium hydroxide concentrations were made and tested to determine the polishing rates and within-wafer non-uniformity.

Example 9: Effect of Alcohol Concentration on Polishing Rates

To determine the effects of alcohol concentration on removal rates of compositions of this invention, we studied three planarization compositions, A, B, anc C with the following compositions and observed removal rates. Thermal oxide wafers were polished using Rodel IC 1400-A1 polishing pad, and a Strasbaugh 6EC CMP tool. The downward force was 8 psi, the table and quill speeds were 150 and 30 rpm, respectively. The slurry flow rate was 200 ml/min at a set point temperature of 25° C.

Slurry Compositions	**A**	**B**	**C**
pH	11.16	10.97	11.02
Ethanol (weight %)	5.72	6.9	2.1
Weight % SiO_2	12.9	12.0	13.4
Particle size(nm)	171	185	178
Polishing Rate (Å/min)	2731	3255	3867

Comparing these results with those of Example 5 show that with high alcohol concentration, the removal rates are lower (1,272 Å/min) than those obtained using compositions with lower alcohol concentrations.

Example 10: Planarization Rates and Wafer Uniformity Using Low Alcohol Compositions

To determine the planarization rates and wafer uniformity obtained using low alcohol compositions of the invention, we polished 50 thermal oxide wafers using a composition with ethanol concentrations below 7 weight %. The results are shown in Figure 4 shows the removal rates (in Å/min) and within-wafer non-uniformity (%) of polishing thermal oxide wafers with the low alcohol planarization compositions of this invention. Fifty wafers were polished, and every fifth was studied. Polishing rates were between 2500 Å/min and 3000 Å/min, which were significantly higher than the polishing rates obtained with high alcohol compositions. Additionally, the within-wafer non-uniformity was below 2 %, which is substantially lower than the wafer non-uniformity observed with high alcohol compositions shown in Table 3.

Therefore, the low alcohol compositions provide higher polishing rates and lower within-wafer non-uniformity than the higher alcohol compositions.

Example 11: Semiconductor Devices Manufactured Using the Planarization Compounds of the Invention

Figure 5 illustrates an embodiment of the present invention depicting a cross-sectional view of a sample semiconductor device **500** made using the method for manufacturing gate structure and inter-layer dielectrics of the present invention before the dielectric film surface has been planarized using the method and composition of the present invention. Layers of gate oxide

516, polysilicon 512 and tungsten silicide 508 are deposited sequentially on top of substrate layer 504. The dielectric film layer 518 has surface 522 with irregularities 526 which are responsible for surface roughness.

Figure 6 illustrates an embodiment of the present invention depicting a cross-sectional view of a sample semiconductor device 600 made using the method for manufacturing gate structure and inter-layer dielectrics of the present invention after the dielectric film surface has been planarized using the method and composition of the present invention. Layers of gate oxide 616, polysilicon 612 and tungsten silicide 608 are deposited sequentially on top of substrate layer 604. The dielectric film layer 618 has surface 622 without surface defects.

Figures 7a and 7b illustrate the planarization of shallow trench isolations 700 of the invention. Figure 7a shows substrate 704 made of bulk Si or epitaxial silicon with shallow trenches 708. A layer of thermal oxide 712 is deposited in the shallow trenches, and optionally, a nitride stop layer 716 is deposited on the top of the substrate 704. A layer of high density plasma oxide 720 is deposited to fill the shallow trenches 708 and cover the nitride stop layer 716.

Figure 7b shows a similar structure 700 as in Figure 7a, but with the surface subjected to CMP of this invention. The substrate 704 has shallow trenches 708 with thermal oxide layers 712. The trenches are filled with high-density plasma oxide 720, and the upper surface 724 is planarized and polished according to the invention, and finally the nitride layer is removed by phosphoric acid treatment.

While the invention has been described in connection with specific embodiments thereof, it will be understood that it is capable of further modification, and this application is intended to cover any variations, uses, or

adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or customary practice in the art to which the invention pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

Industrial Applicability

The present invention provides compositions for chemical mechanical planarization and methods of using the compositions to remove interlayer dielectric materials from the surfaces of semiconductor wafers following deposition of thin films such as tungsten silicide/polysilicon/gate structures or titanium/aluminum/titanium nitride stacks. Advantageously, the method of the present invention provides a interlayer dielectric surface that has less surface roughness, is higher purity and reduces scratch density. The present invention also provides articles of manufacture such as semiconductor devices made incorporating the improved planarization methods. The improvements in the planarity of semiconductor devices is extremely important to the semiconductor industry wherein extreme precision and surface cleanliness on a nanometer scale is essential to the manufacture of high density semiconductor devices, with high manufacturing throughput.

We Claim:

1. A planarization composition having a pH from about 9 to about 11.5, comprising an alkosol comprising:

spherical, monodisperse alkylsilicate particles, and

a liquid carrier comprising:

an alcohol, in the range of about 0 weight % to about 9 weight %,

a base, and

the remainder, water.

2. The planarization composition of claim 1, wherein the spherical alkylsilicate particles have diameters in the range of about 30 nm to about 400 nm.

3. The planarization composition of claim 1, wherein the monodispersity of the alkylsilicate particles is such that at least about 90 weight % of the particles have diameters which are no more than about 20 % different from the weight average diameter.

4. The planarization composition of claim 1, wherein the alkylsilicate particles are present in amounts ranging from about 0.5 weight % to about 30 weight %.

5. The planarization composition of claim 1, wherein the base is selected from the group consisting of potassium hydroxide, and an amine hydroxide selected from the group consisting of ammonium hydroxide, NR_4OH and

NR_2NR_3OH, wherein each R is independently selected from the group consisting of H, CH_3, CH_2CH_3, C_3H_7, and C_4H_9.

6. The planarization composition of claim 5, wherein the hydroxyl amine concentration is in the range of about 0.2 weight % to about 9 weight %.

7. The planarization composition of claim 5, wherein the hydroxyl amine concentration is in the range of about 0.2 weight % to about 4 weight %.

8. A planarization composition having a pH from about 9 to about 11.5, comprising an alkosol comprising:

from about 0.5 weight % to about 30 weight % of spherical alkylsilicate particles having a weight average particle diameter in the range of about 30 nm to about 400 nm, and is mono-disperse in that at least about 90 weight % of the particles have diameters which are no more than about 20 % different from the weight average diameter, and

a liquid carrier comprising:

an alcohol, in the range of about 0 weight % to about 9 weight %,

at least one base selected from the group consisting of potassium hydroxide and an amine hydroxide selected from the group consisting of ammonium hydroxide, NR_4OH and NR_2NR_3OH, wherein each R is independently selected from the group consisting of H, CH_3, CH_2CH_3, C_3H_7, and C_4H_9 in an amount in the range of about 0.2 weight % to about 9.0 weight %, and

the remainder water.

9. The planarization composition of claim 1, wherein the pH is adjusted by adding at least one of an acid selected from the group consisting of nitric, sulfuric, hydrochloric, carboxylic, acetic, citric, acetylsalicylic, and dicarboxylic acids.

10. The planarization composition of claim 1, wherein the pH is adjusted by controlling the concentration of at least one of said base.

11. The planarization composition of claim 1, wherein the total dissolved metal content is no more than about 20,000 parts per billion.

12. The planarization composition of claim 1, wherein the total dissolved metal content is no more than about 2000 parts per billion.

13. The planarization composition of claim 1, wherein the total dissolved metal content is no more than about 500 parts per billion.

14. The planarization composition of claim 1, wherein the concentration of at least one of said alcohol and said base is adjusted after the formation of alkylsilicate particles.

15. The planarization composition of claim 1, wherein the concentration of at least a base is adjusted after the formation of alkylsilicate particles.

16. The planarization composition of claim 1, wherein the concentration of a first base is decreased after the formation of alkylsilicate particles, and the concentration of a second base is increased after the formation of alkylsilicate particles.

17. The planarization composition of claim 1, wherein the planarization rates on borophosphoroustetraethylorthosilicate glass (BPTEOS) are in the range of about 500 Å per min to about 15,000 Å per min.

18. The planarization composition of claim 1, wherein the planarization rates on borophosphoroustetraethylorthosilicate glass (BPTEOS) are in the range of about 3000 Å per min to about 15,000 Å per min.

19. The planarization composition of claim 1, wherein the planarization rates on thermal oxide are in the range of about 500 Å per min to about 10,000 Å per min.

20. The planarization composition of claim 1, wherein the pH of said composition is in the range of about 10 to about 11.5.

21. The planarization composition of claim 1, wherein the pH of said composition is in the range of about 10 to about 11.

22. The planarization composition of claim 1, wherein the root mean square surface roughness of a planarized surface is less than about 20 Å.

23. The planarization composition of claim 1, wherein the root mean square surface roughness of a planarized surface is less than about 10 Å.

24. The planarization composition of claim 1, wherein the root mean square surface roughness of a planarized surface is less than about 5 Å.

25. The planarization composition of claim 1, wherein the alkylsilicate particles are synthesized from a tetraalkylsiloxane.

26. The planarization composition of claim 1, wherein the alkylsilicate particles are synthesized from a tetraalkylsiloxane, wherein said tetraalkylsiloxane comprises alkyl moieties selected independently from the group consisting of methyl, ethyl, butyl, isobutyl, propyl, and isopropyl moieties.

27. The planarization composition of claim 1, wherein the alkylsilicate particles are synthesized from tetraethylorthosilicate (TEOS).

28. A method for manufacturing an alkosol planarization composition, comprising:

hydrolyzing an tetraalkylsiloxane precursor in a solution comprising:

at least one alcohol, in an amount in the range of about 30 weight % to about 45 weight %,

at least one base, such that the pH of the solution is in the range of about 7 to about 11.5,

the remainder, water,

allowing the hydrolyzed tetraalkylsiloxane precursor to form spherical alkylsilicate particles,

adjusting, after the formation of said alkylsilicate particles, the concentration of said alcohol, and optionally,

adjusting at least one of the pH and the concentration of at least one of said base after the formation of said alkylsilicate particles.

29. The method of claim 28, wherein the at least one base is selected at least one base selected from the group consisting of potassium hydroxide and an amine hydroxide selected from the group consisting of ammonium hydroxide, NR_4OH and NR_2NR_3OH, wherein each R is independently selected from the group consisting of H, CH_3, CH_2CH_3, C_3H_7, and C_4H_9.

30. The method of 29, wherein the concentration of at least one of said base is in the range of about 0.2 weight % to about 9 weight %.

31. A method for manufacturing an alkosol planarization composition, comprising:

hydrolyzing an tetraalkylsiloxane precursor in a solution comprising:

at least one alcohol, in an amount in the range of about 30 weight % to about 45 weight %,

at least one base selected from the group consisting of potassium hydroxide and an amine hydroxide selected from the group consisting of ammonium hydroxide, NR_4OH and NR_2NR_3OH, wherein each R is independently selected from the group consisting of H, CH_3, CH_2CH_3, C_3H_7, and C_4H_9 in an amount in the range of about 0.2 weight % to about 9.0 weight %, and

the remainder water, wherein the pH of the solution is between about 9 and about 11.5,

allowing the hydrolyzed tetraalkylsiloxane precursor to form spherical alkylsilicate particles, and optionally,

adjusting at least one of the pH, an alcohol and a base of the planarization composition.

32. The method of claim 31, wherein the pH of said composition is adjusted to the range of about 10 to about 11.5.

33. The method of claim 31, wherein the pH of said composition is adjusted to the range of about 10.5 to about 11.

34. The method of claim 31, additionally comprising adjusting the content of at least one of an alcohol and a base in the planarization composition after the formation of alkylsilicate particles.

35. The method of claim 34, wherein the method for adjusting the content of an alcohol in the planarization composition after the formation of alkylsilicate particles is selected from the group consisting of evaporation and ultrafiltration.

36. The method of claim 34, wherein the concentration of a first base consisting of an amine hydroxide is reduced, and the concentration of a second base is increased.

37. The method of claim 34, wherein the method for adjusting the content of an alcohol is ultrafiltration.

38. The method of claim 37, wherein the ultrafiltration is accomplished using apparatus, wherein surfaces of said apparatus exposed to planarization chemicals comprise materials selected from the group of stainless steel and titanium oxide.

39. The method of claim 38, wherein the stainless steel is type 316 stainless steel.

40. The method of claim 37, wherein the temperature of the ultrafiltration apparatus is in the range of about 20° C to about 80° C.

41. A planarization apparatus, comprising:

a pad adapted to be frictionally moved across a surface, said pad having between it and the surface a planarization composition as set forth in any of claims 1 to 27.

42. A method of planarizing a substrate having at least one coating, comprising the steps of:

positioning the planarization composition of any of claims 1 to 21 between a pad and the at least one coating, wherein the at least one coating comprises a dielectric material; and

rubbing the pad against the at least one coating until the at least one coating has been at least partially planarized.

43. The method of claim 42, wherein the root mean square surface roughness of the planarized surface coating has been improved to less than about 20 Å.

44. The method of claim 42, wherein the root mean square surface roughness of the planarized surface coating has been improved to less than about 10 Å.

45. The method of claim 42, wherein the root mean square surface roughness of the planarized surface coating has been improved to less than about 5 Å.

46. The method of claim 42, wherein the substrate surface is on a wafer, wherein the non-uniformity of the planarized wafer is in the range of about 0 % to about 10 %.

47. The method of claim 42, wherein the substrate surface is on a wafer, wherein the non-uniformity of the planarized wafer is in the range of about 0 % to about 5 %.

48. The method of claim 42, wherein the substrate surface is on a wafer, wherein the non-uniformity of the planarized wafer is less than about 5 %.

49. The method of claim 42, wherein the substrate surface is on a wafer, wherein the non-uniformity of the planarized wafer is less than about 2 %.

50. The method of claim 42, wherein the planarization rates on borophosphoroustetraethylorthosilicate glass (BPTEOS) are in the range of about 500 Å per min to about 15,000 Å per min.

51. The method of claim 42, wherein the planarization rates on borophosphoroustetraethylorthosilicate glass (BPTEOS) are in the range of about 3000 Å per min to about 15,000 Å per min.

52. The method of claim 42, wherein the planarization rates on thermal oxide are in the range of about 500 Å per min to about 10,000 Å per min.

53. The method of claim 42, wherein the at least one coating is selected from the group consisting of undoped silicon dioxide and doped silicon dioxide.

54. The method of claim 53, wherein the at least one coating is selected from the group consisting of boron phosphorous doped silicate glass (BPSG), phosphorous doped silicate glass (PSG), phosphorous-doped tetraethylorthosilicate glass (PTEOS), thermal oxides, plasma-enhanced tetraethylorthosilicate (PTEOS) glass, and high density plasma chemical vapor deposited (HDPCVD) glass.

55. The method of claim 42, wherein the at least one coating is selected from the group consisting of a CMP stop layer, a silicide and barrier layer.

56. The method of claim 55, wherein the stop layer is a silicon nitride.

57. The method of claim 55, wherein the barrier layer is selected from the group consisting of titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride and titanium/tungsten.

58. The method of claim 55, wherein the silicide is selected from the group consisting of tantalum silicide, titanium silicide and tungsten silicide.

59. A method for manufacturing a semiconductor device comprising an interlayer dielectric material, comprising the steps of:

providing a substrate with a first dielectric surface,

depositing a patterned photoresist layer on said first surface, whereby the first dielectric layer is at least partially exposed,

etching one or more small holes defined by respective sidewalls and bottoms into said second surface,

removing the photoresist layer, thereby exposing the first dielectric layer,

depositing a barrier layer into at least one of said small holes in said dielectric layer and onto the respective sidewalls of at least one of said small holes,

depositing a metal layer on top of said barrier layer,

depositing a second layer of dielectric material,

positioning the planarization composition of any of claims 1 to 27 between said second layer of dielectric material and a polishing pad, and

rubbing the pad against said second dielectric layer sufficiently to thin and at least partially planarize the second dielectric layer.

60. A method for manufacturing a semiconductor chip comprising a shallow trench isolation, comprising:

providing a substrate,

patterning said substrate with photoresist, leaving portions of the substrate exposed,

etching the substrate, forming at least one small hole,

growing a first layer of a first dielectric material, thereby coating the inside sidewalls and bottom of at least one hole,

depositing of a second layer of second dielectric material, which substantially fills said at least one hole, and

thinning and substantially planarizing the dielectric layers using the planarization composition of at least one of claim 1 to 27, thereby exposing the substrate.

61. A method of manufacturing a semiconductor chip comprising an electrically isolated gate structure, comprising:

providing at least one gate structure and another electrical element,

depositing a layer of dielectric material between and onto said gate structure and electrical element, and

planarizing said dielectric using the planarization composition of any of claims 1 to 27.

62. A semiconductor chip wherein at least one element has been planarized using the planarization composition of any of claims 1 to 27.

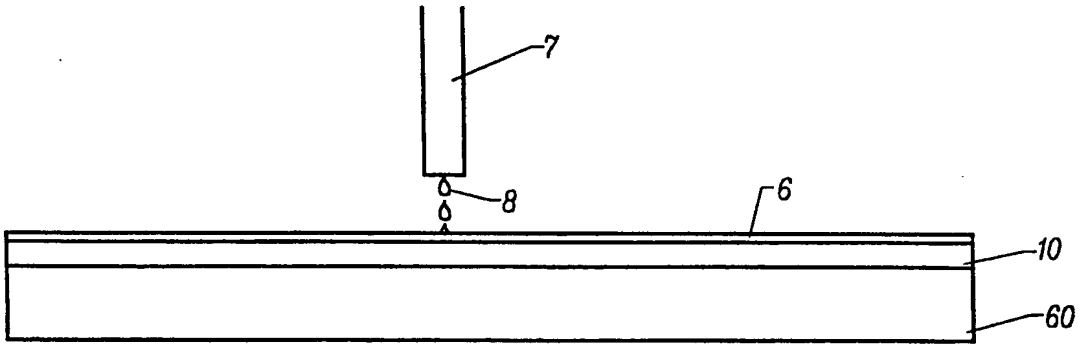


FIG. 1

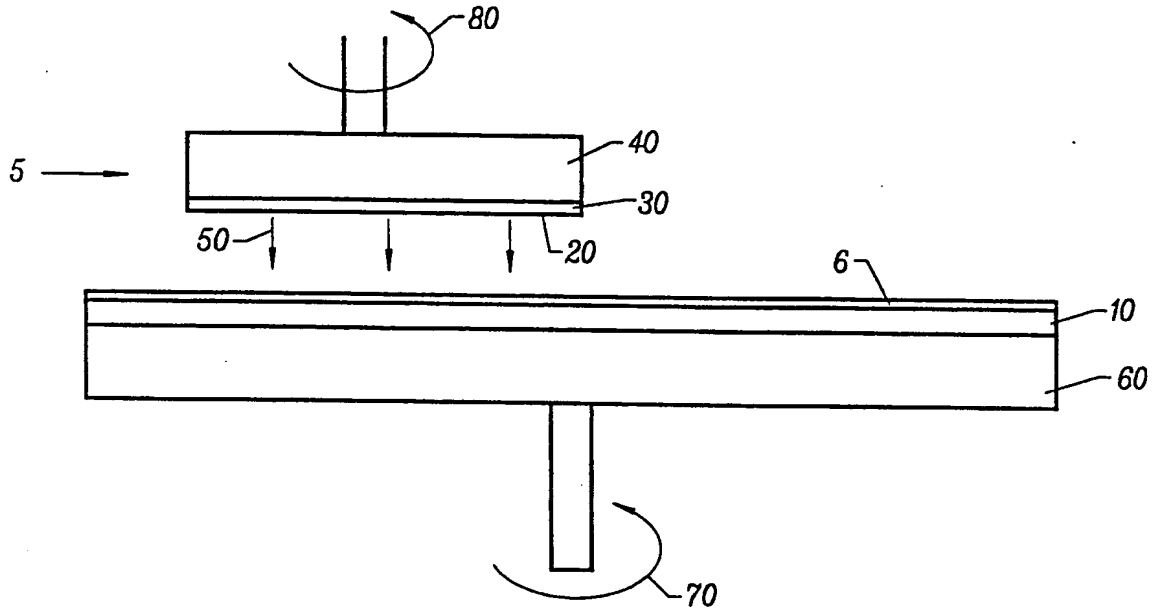
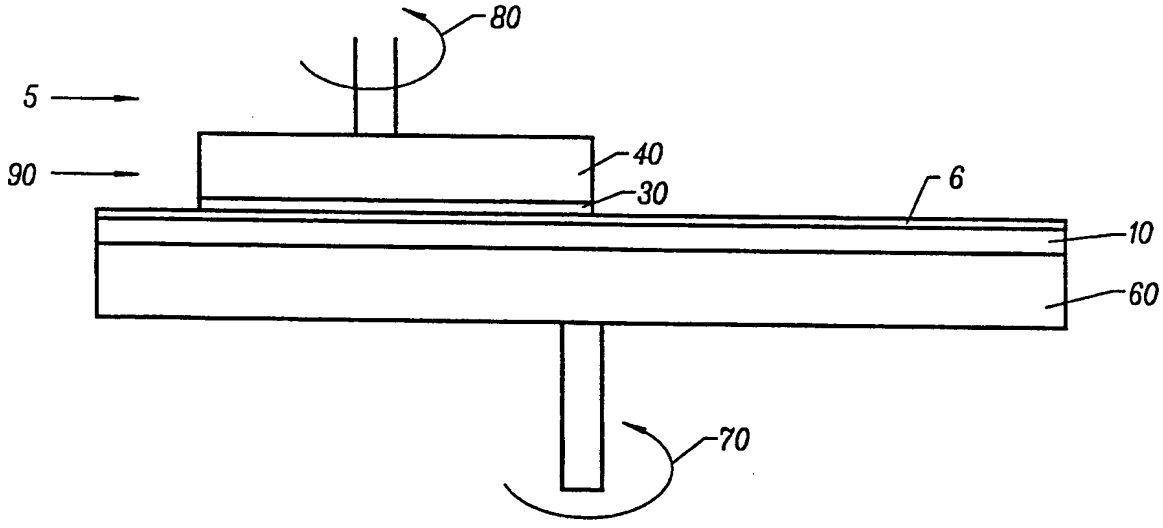


FIG. 2



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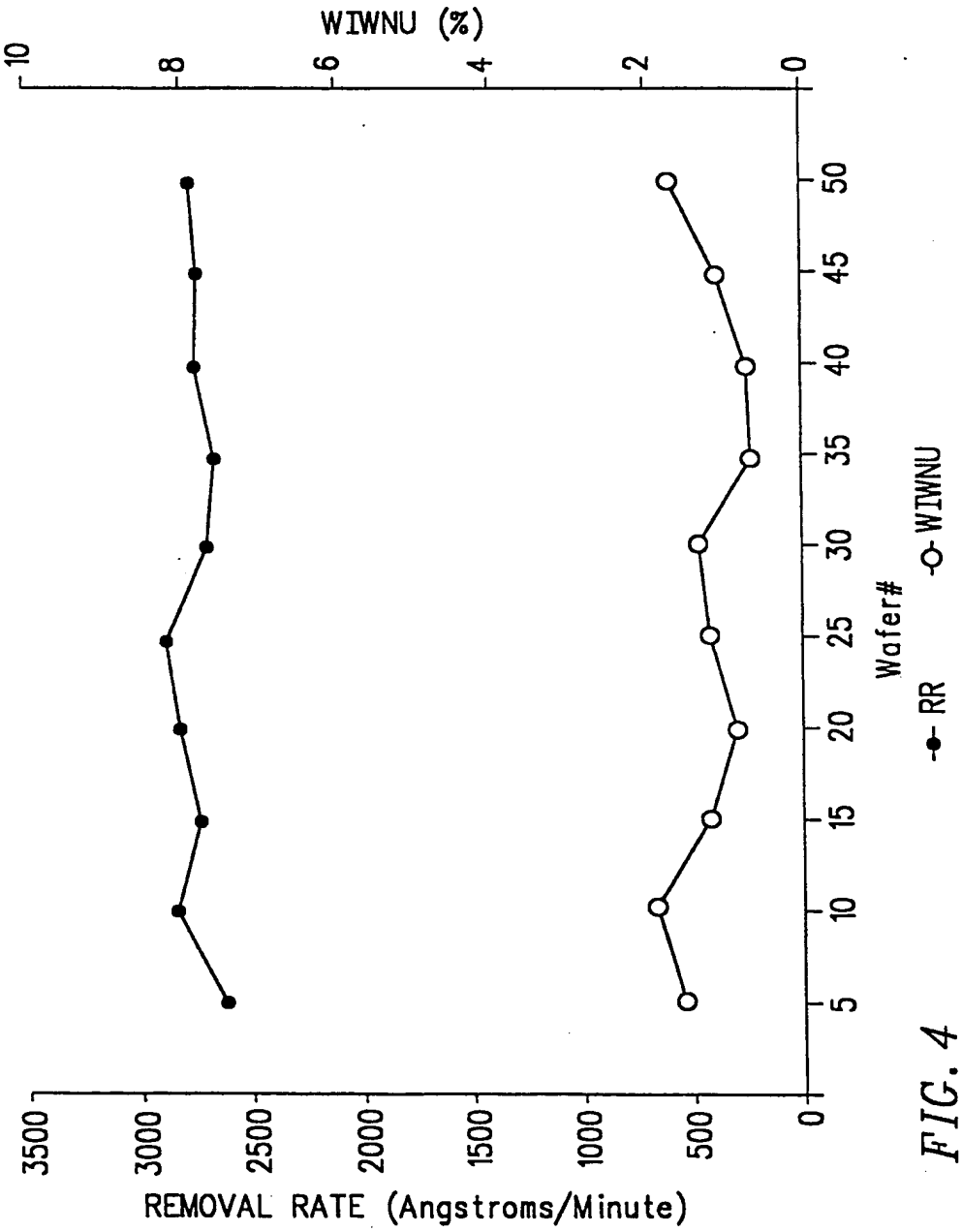
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8
6
4
2
0
3500
3000
2500
2000
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1000
500
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Wafer#
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FIG. 4

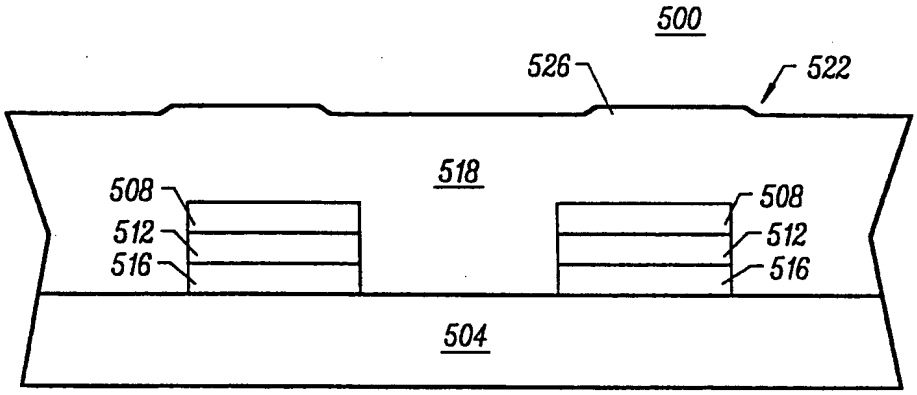
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FIG. 5

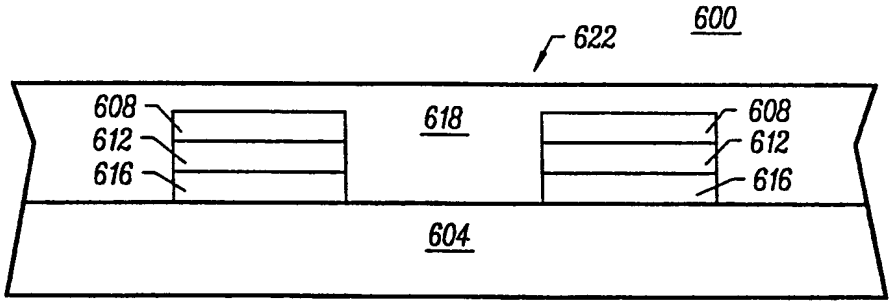
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FIG. 6

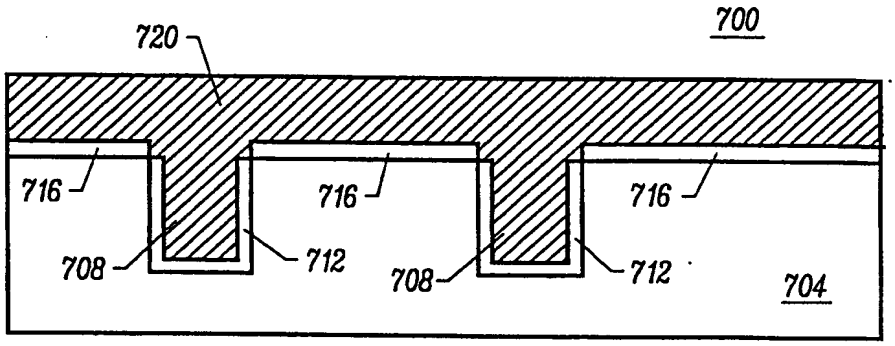
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FIG. 7a

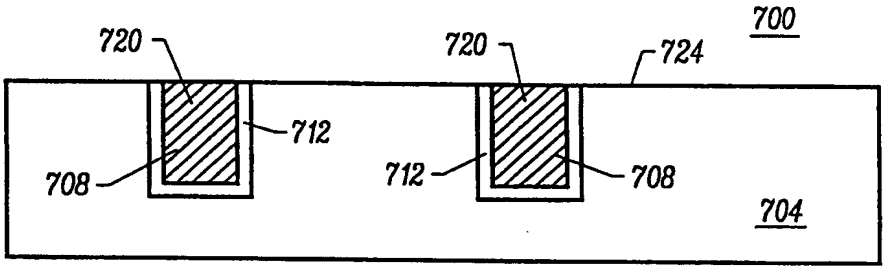
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FIG. 7b

INTERNATIONAL SEARCH REPORT

Inte tional Application No
PCT/US 98/08107

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/3105 C09G1/02 C09K3/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L C09G C09K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	STOBER W ET AL: "CONTROLLED GROWTH OF MONODISPERSE SILICA SPHERES IN THE MICRON SIZERANGE" JOURNAL OF COLLOID AND INTERFACE SCIENCE, vol. 26, 1 January 1968, pages 62-69, XP000561462 see the whole document ---	1,8, 28-31
A	US 5 230 833 A (ROMBERGER JOHN A ET AL) 27 July 1993 see the whole document --- -/--	1,2,4,8, 11-13, 15,28, 31-33, 41,42, 59-62

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 1998	11/08/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Inte 'onal Application No
PCT/US 98/08107

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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1

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Information on patent family members

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